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09/650,726	08/30/2000	Denis Miglianico	Q60462	1213

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,726	MIGLIANICO, DENIS	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006 and 28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicant's Amendment ("Amendment") to Office Action dated August 30, 2005, mailed January 30, 2006, and Applicant's Response ("Response") and RCE to Advisory Action dated February 24, 2006, mailed February 28, 2006.

1-1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 30, 2006, has been entered.

1-2. Claims 1, 5, and 7 have been amended. Claims 1-3 and 5-10 are pending.

1-3. Claims 1-3 and 5-10 have been examined and rejected.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-3 and 5-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3-1. The amended independent claim 1 recites the limitation, "receiving low output signals from said unit" in line 3 of the claim, and the amended independent claim 5 recites the same limitation in line 5 of the claim, which does not appear to have support in the original disclosure. For example, as described in the specification at page 7, lines 19-21, "The output signals S generated by the unit 1 comprise fast signals S_1, relatively slow signals S_2, and analog signals S_3". Therefore, "receiving low output signals from said unit" does not appear to have support in the original disclosure. Applicant argues, "support for the claim amendments can be found at page 7, line 17 to page 8, line 8 of specification and in figure 1, for example" (page 2, paragraph 1, Response). However, the Examiner has not been able to locate the alleged support.

3-2. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5-1. Claim 8 recites the limitation "said second programmable logic circuit" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5-2. Claim 10 recites the limitation "said second programmable logic circuit" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Interpretation

6. Independent claims 1 and 5 recite the limitation "receiving low output signals from said unit" in each claim. However, it does not appear to have support in the specification, as discussed in section 3-1 above. For the purpose of claim examination with the broadest reasonable interpretation, the Examiner will presume that any output signal is qualified as a "low output signal" assuming a high threshold in defining the "low output signal".

Recommendations

7. Claim 1 recites the limitation "input signals" in line 3 and "said input simulation signals" in lines 4 and 5 of the claim. For clarification purpose, the Examiner suggests that "input signals" in line 3 be replaced with "simulated input signals" and "said input simulation signals" in lines 4 and 5 be replaced with "said simulated input signals".

8. Claim 2 recites the limitation "switching instants of logic signals" in line 2 of the claim. For clarification purpose, the Examiner suggests that "switching instants of logic signals" be replaced with "said fast output signals".

9. Claim 5 recites the limitation "receives at least fast output signal" in lines 7-8 of the claim. For clarification purpose, the Examiner suggests that "receives at least fast output signal" be replaced with "receives at least one of fast output signals".

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-3, 5-7, and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hanselmann, "Real-Time Simulation Replaces Test Drives", Test and Measurement World, February 15, 1996, pages 35-36, 38, 40.

11-1. Regarding claim 1, Hanselmann discloses a method of testing the operation of an electronic unit (electronic control unit, page 35, FIGURE 1) by stimulating said unit with simulated input signals to said unit, the method comprising:

- sending input signals to said unit (for example, Engine Speed and Engine Torque, page 35, FIGURE 1) and receiving low output signals from said unit in response to said input simulation signals (for example, Torque Command or Pressure Sensors output, page 35, FIGURE 1) by at least one microprocessor (multiple digital signal processors, page 36, left column, paragraph 1);

- receiving fast output signals in response to said input simulation signals (for example, Torque Command, page 35, FIGURE 1) by at least one programmable logic circuit (DDS board, page 36, right column, paragraph 3); and

- processing the fast output signals by the at least one logic circuit to generate parameter values at a first frequency (compute signals on-line, page 36, right column, paragraph 3);

- storing said parameter values corresponding to said processed signals in a storing circuit (upload them to the MATLAB workspace, page 38, center column, last paragraph); and

- accessing said stored parameter values by the at least one microprocessor at a second frequency which is slower than said first frequency and is compatible with an operating

frequency of the microprocessor that generates said simulated input signals (DSP generate signals much faster than the vehicle simulation, page 36, right column, paragraph 3).

11-2. Regarding claim 2, Hanselmann further discloses said parameter values are representative of switching instants of logic signals generated by said unit (Torque Command, page 35, FIGURE 1).

11-3. Regarding claim 3, Hanselmann further discloses said parameter values are an image of said switching instants, of the duration during which a logic variable has a predetermined value, and/or the mean value of a logic variable over a predetermined period (postprocessing, page 38, right column, paragraph 2).

11-4. Regarding claim 5, Hanselmann discloses an apparatus for testing the operation of an electronic unit (electronic control unit, page 35, FIGURE 1) by simulation, said unit generating logic signals at specific instants, said apparatus comprising a simulator (Simulator, page 35, FIGURE 1) which comprises:

- at least one microprocessor (for example, Master DSP, page 35, FIGURE 1) sending input simulation signals to said unit (electronic control unit, page 35, FIGURE 1) and receiving low output signals from said unit in response to said input simulation signals (for example, Torque Command or Pressure Sensors output, page 35, FIGURE 1);

- at least one programmable logic circuit (DDS board, page 36, right column, paragraph 3) which receives at least fast output signal from said unit, said logic circuit processing the fast output signals to generate, at a first frequency, parameter values corresponding to the fast output signals (compute signals on-line, page 36, right column, paragraph 3); and

- a storing circuit which stores said parameter values (upload them to the MATLAB workspace, page 38, center column, last paragraph), wherein said microprocessor accesses said stored parameter values at a second frequency which is slower than said first frequency and is compatible with an operating frequency of said microprocessor (DSP generate signals much faster than the vehicle simulation, page 36, right column, paragraph 3).

11-5. Regarding claim 6, Hanselmann further discloses comprising at least one second programmable logic circuit which sends in real time simulation signals to said unit on the basis of reference signals previously issued by said microprocessor (DDS board contains its own DSPs, page 36, right column, paragraph 3).

11-6. Regarding claim 7, Hanselmann further discloses said programmable logic circuit which receives said at least one of said fast output signals and said second programmable logic circuit which sends simulation signals to said unit are implemented as a single electronic circuit (DDS board, page 36, right column, paragraph 3).

11-7. Regarding claim 9, Hanselmann further discloses said simulator further comprises at least one of:

an analog-to-digital converter which forward digital signals representative of analog signals generated by said unit to said microprocessor, and a digital-to-analog converter which forwards analog simulation signals based on digital signals generated by said microprocessor to said unit (digital-to-analog converter, page 36, right column, paragraph 2).

11-8. Regarding claim 10, Hanselmann further discloses at least one of said programmable logic circuit and said second programmable logic circuit is programmed as a function of the type

and/or intended use of said unit (Generating wheel-speed signal, page 36, right column, paragraph 4).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanselmann, "Real-Time Simulation Replaces Test Drives", Test and Measurement World, February 15, 1996, pages 35-36, 38, 40, in view of Turner, U.S. Patent 6,269,020 B1 issued July 31, 2001, and filed February 5, 1999.

13-1. Regarding claim 8, Hanselmann fails to disclose at least one of said programmable logic circuit and said second programmable logic circuit is of the field programmable gate array type.

Turner discloses, as shown in FIG. 1, a processing unit incorporates a programmable logic device and the processing unit may be a DSP (Turner, column 1, lines 40-60). Turner further discloses, "Programmable logic devices (sometimes referred to as a PALs, PLAs, FPLAs, PLDs, EPLDs, EEPLDs, LCAs, or FPGA), are well-known integrated circuits that provide the advantages of fixed integrated circuits with the flexibility of custom integrated circuits. Such devices allow a user to electrically program standard, off-the-shelf logic elements to meet a user's specific needs" (Turner, column 1, lines 22-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hanselmann to incorporate the teachings of Turner to obtain the invention as specified in claim 8 because FPGA is well-known and allows a user to electrically program standard, off-the-shelf logic elements to meet a user's specific needs.

Applicant's Arguments

14. Applicant argues the following:

(1) "In particular, these passages do not disclose that one of the multiple DSPs (i.e. the DDS or the parallel processing DSP) receives fast output signals from the unit under test" (page 6, paragraph 1, Amendment).

(2) "So, the digital-to-analog converter DDS produces analog signals for the unit under test, but it does not receive and process fast output signals received from the unit under test" (page 6, paragraph 2, Amendment).

(3) "The parallel processing DSP does not process the fast output signals from the unit under test" (page 6, paragraph 3, Amendment).

(4) "it does not disclose that a logic circuit (DDS, parallel processing DSP) processes fast output signals and stores them in a memory and that a microprocessor 14 (Master DSP) processes low signals and accesses the processed fast output signals in the memory 19 at its own frequency" (page 7, paragraph 1, Amendment).

(5) "Hanselmann does not disclose that the duration of the vehicle simulation corresponds to the time between two accesses of the microprocessor 14 (Master DSP) to the memory of the logic circuit 18 (DDS, parallel processing DSP)" (page 7, paragraph 2, Amendment).

(6) "This paragraph does not disclose that the Master DSP accesses the parameter values stored in the memory 19 of the logic circuit 18 (DDS, parallel processing DSP)" (page 8, paragraph 1, Amendment).

(7) "Applicant submits that dependent claim 8 is allowable at least by virtue of its dependency from independent claim 5" (page 8, paragraph 2, Amendment).

Response to Arguments

15. Applicant's arguments have been fully considered.

15-1. Applicant's arguments (1) - (7) are not persuasive. First, as discussed in section 3-1 above, the limitation "low output signals" does not appear to have support in the specification. For the purpose of claim examination with the broadest reasonable interpretation, the Examiner has presumed, in section 6 above, that any output signal is qualified as a "low output signal" assuming a high threshold in defining the "low output signal". Therefore, all signals disclosed in Hanselmann reference meet the claimed "low output signals" and "fast output signal". Second, as described at page 36, column 1, paragraph 1, Hanselmann et al. disclose, "The gray box on the left contains the real-time hardware for the test bench - multiple digital signal processors (DSPs), I/O boards, and interfacing circuitry" and "The real-time hardware handles all closed-loop computing, which has to meet stringent time requirements". Accordingly, at least one of the multiple DSPs (programmable logic circuits) has to receive at least one of the output signals from the unit under test and generate parameter values corresponding to the received signals in order to meet the requirement - "the real-time hardware handles all closed-loop computing". Third, as described at page 36, column 3, paragraph 3, Hanselmann et al. disclose the DSP

generates signals much faster than the vehicle simulation. In other words, the DSP receives the output signals and generate parameter values at a frequency that is greater than an accessing frequency. Therefore, storing the generated parameter values and waiting for the processing by the Master DSP is necessary.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
March 18, 2006 H.D.

Thai Phan
Art unit 2128